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Lecture - 11 Oxidation I - Kinetics of Oxidation Silicon on Insulator | L 22 | VLSI Technology | IC Fabrication | ESE NET |

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Photolithography: Step by step

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The SiO<sub>2</sub> is etched and an arsenic implant forms the N<sup>+</sup> regions. SILICON VLSI TECHNOLOGY Fundamentals, Practice and Modeling By Plummer, Deal and Griffin 30 © 2000 by Prentice Hall Upper Saddle River, NJ. fSolutions Manual N<sup>+</sup> N<sup>+</sup> P P<sup>+</sup> P<sup>+</sup> N N<sup>+</sup> P The N<sup>+</sup> regions are driven-in to their final junction depth.

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Silicon-On-Insulator (SOI) CMOS technology has been regarded as another major technology for VLSI in addition to bulk CMOS technology. Owing to the buried oxide structure, SOI technology offers superior CMOS devices with higher speed, high density, and reduced second order effects for deep-submicron low-voltage, low-power VLSI circuits ...

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Solutions Manual SILICON VLSI TECHNOLOGY 10 © 2000 by Prentice Hall Fundamentals, Practice and Modeling Upper Saddle River, NJ. By Plummer, Deal and Griffin P N+ The buried layer is driven in using a high temperature furnace cycle. P N+ N The SiO<sub>2</sub> is etched off the surface and an N type epitaxial layer is grown. Note that

## ~~S G D S G D N P N N P N P WELL P+~~

Text: Silicon VLSI Technology: Plummer, Deal and Griffin Prerequisite: EE/MSE486 (Fundamentals of Integrated Circuit Technology) or EE/MSE 502 (Introduction to MEMS) or EE 527 (Solid State Laboratory Techniques) or equivalent exposure to basics of photolithography and diffusion/reaction problems, or consent of instructor.

## ~~EE/MSE 528 Physics and Modeling of VLSI Fabrication~~

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